Advance Program (Dated 31-10-2006)

First International Workshop on Interconnect Design and Variability

December 28-29, 2006, Bangalore, India

Venue: Golden Jubilee Hall, ECE Dept, IISc, Bangalore, India

Organized by

http://vlsi-india.org/vsi

VLSI Society of India

In cooperation with

Indian Institute of Science, Bangalore, India

Indian Institute of Science, Bangalore

IEEE Circuits and Systems Society Bangalore Chapter

http://www.ieee.org

IDV 2006

Scope of the Workshop

Interconnect scaling and variability are two difficult challenges in sub-100nm technology nodes. This workshop aims at addressing the following topics.

1. **Latest advances in interconnect modeling and design innovations to continue performance scaling in sub-100nm technologies:**
   - Technology scaling trends
   - New process realities in sub-100nm technologies
   - Alternative interconnect methods
   - Interconnect analysis algorithms
   - Design and Architecture methods to mitigate RC scaling
2. **In depth review of the latest advances in variability in sub-100nm technologies:**
   - Device and interconnect process variations
   - Algorithms related to statistical analysis of performance and leakage
   - Practical approaches to address variability
   - Variation tolerant design methods

General Co-Chairs:

Nagaraj, N.S. Texas Instruments (Dallas)

C.P. Ravikumar, Texas Instruments (Bangalore)

Program Committee:

- **Andrzej Strojwas**, Carnegie Mellon University, USA
- **Dipu Pramanik**, Synopsys, USA
- **Jaijeet Roychowdhury**, Univ. of Minnesota, USA
- **Krishna Saraswat**, Stanford University, USA
- **Larry Pileggi**, Carenegie Mellon University, USA
- **Nickhil Jakatdar**, Cadence Design Systems, USA
- **Poras Balsara**, Univ. of Texas at Dallas, USA
- **Ram Achar**, Carleton University, Canada
- **Sachin Sapatnekar**, Univ. of Minnesota, USA
- **Yervant Zorian**, Virage Logic, USA

Speakers:

1. **Dr. Jaijeet Roychowdhury**, University of Minnesota, USA
2. **Dr. Krishna Saraswat**, Stanford University, USA
3. **Dr. Ram Achar**, Carleton University, Canada
4. **Dr. Shankar Balachandran**, IIT Madras, Chennai, India
5. **Vijay Sindagi**, Texas Instruments, India
6. **Dr. Andrzej Strojwas**, Carnegie Mellon University, USA
7. **Dr. Dipu Pramanik**, Synopsys, USA
8. **Dr. Mustafa Celik**, Extreme DA, USA
9. **Dr. Nickhil Jakatdar**, Cadence Design Systems, USA
10. **Dr. Sarma Vrudhula**, Arizona State Univeristy, USA
11. **Dr. Vivek De**, Intel, USA

Course Fee	Before November 28, 2006	After November 28, 2006
Professionals (Non-members)	**Rs. 4,000**	**Rs. 4,500**
Professionals (VSI/ IEEE members)	**Rs. 3,000**	**Rs. 3,500**
Students/Faculty (Non-members)	**Rs. 2,500**	**Rs. 3,000**
Students/Faculty (VSI/ IEEE members)	**Rs. 2,000**	**Rs. 2,500**

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First International Workshop on Interconnect Design and Variability

Program Schedule

Day-1 - December 28, 2006:

Interconnect RC parameters are significant components of circuit performance, signal integrity and reliability in IC design. Due to manufacturability and reliability issues, the effective dielectric constant of the inter-metal dielectric is not scaling commensurate with the technology scaling predicted in the ITRS roadmap. Metal resistance is also increasing due to electron scattering effects, which exacerbates the interconnect RC scaling issues in sub-100nm technology nodes. The increase in contact and via resistance further aggravates the technology entitlement issues. Although reverse scaling is an attractive option for high performance designs, area entitlement is an issue in routing limited designs. Overall improvement in interconnect performance relies more and more on architecture & design techniques and novel interconnect schemes. The sessions on Day 1 review interconnect scaling, signal integrity, physical design, architecture solutions and optical interconnect.

Speakers:

1. **Dr. Jaijeet Roychowdhury**, University of Minnesota
2. **Dr. Krishna Saraswat**, Stanford University, USA
3. **Dr. Ram Achar**, Carleton University, USA
4. **Dr. Shankar Balachandran**, IIT Madras, Chennai, India
5. **Vijay Sindagi**, Texas Instruments, Bangalore, India

The day will close with a panel discussion.

Day-2 - December 29, 2006:

Design For Manufacturability Yield (DFM&Y) has received much attention in sub-100nm technologies. Addressing the challenges in systematic and random process variations is a critical part of the DFM&Y strategy. Global and local variations in transistors have been analyzed in analog circuits for several years and recently extended to large-scale digital circuits in the form of Statistical Static Timing Analysis (SSTA). In additional to random variations, systematic variations such as stress induced variations need to be considered. In addition to transistor variations, interconnect variations due to Chemical Mechanical Polishing (CMP), etch and process bias are important considerations. Structured layout, variation-aware and variation tolerant design techniques help mitigate variability issues. The sessions on Day 2 review key aspects of lithography, CMP, etch and stress induced variations, SSTA methods and variation tolerant design techniques.

Speakers:

1. **Dr. Andrzej Strojwas**, Carnegie Mellon University, USA
2. **Dr. Dipu Pramanik**, Synopsys, USA
3. **Dr. Mustafa Celik**, Extreme DA, USA
4. **Dr. Nickhil Jakatdar**, Cadence Design Sytems, USA
5. **Dr. Sarma Vrudhula**, Arizona State Univeristy, USA
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	Academic/governmental organization from India (VSI/ IEEE member)	☐	VSI/ IEEE Membership No:	

If you are a student, mention Semester/Year:

Contact Address: (Provide permanent mailing address)	**Designation:** Student ☐ Faculty ☐ Industry ☐ Other ☐ **College/ Company:** **Permanent address:**			
E-mail: (Compulsory)				
Background in VLSI: (Courses/Reading/Projects)				
Details of DD enclosed	Amount		DD Number	
	Drawn on Bank		Dated	

Your background and expectations from the workshop:

Signature

After completing the registration form, mail it with the DD to the following address:

Mr. Gopal Naidu
Treasurer, VLSI Society of India
Finance Department
Texas Instruments (India) Pvt Ltd
Bagmane Tech Park
C.V. Raman Nagar, Bangalore
560093

Please do not send scanned copies of DD by mail.

- *The DD to be made out to "**VLSI Society of India**" payable at **Bangalore**.*
- *On the back of the DD, please write "**Interconnect Design and Variability 2006 – Bangalore**".*
- *Partial registration not permitted. No returns will be made against cancellation – the materials will be mailed to your contact address if you cancel.*
- *Queries may please be sent to: vsisecy@vlsi-india.org*
- ***Venue:** Golden Jubilee Hall, ECE Dept, IISc, Bangalore, India.*
- *Course fee includes registration material, lunch and refreshments on all the days.*
- *Transport and stay arrangements are the responsibility of the participants.*
- *Registration can be transferred to a colleague with 15 days prior intimation.*
- *Registration: 8.30 AM Course: 9.00 – 6.00 PM*

Please enter the details in the online registration form at http://vlsi-india.org/vsi/activities/reg.shtml apart from sending the filled hardcopy.